PATENT COOPERATION TREATY

From the:
INTERNATIONAL SEARCHING AUTHORITY

To:

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PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Applicant's or agent's file reference 20500300KC	Date of mailing *(day/month/year)* 27 APR 2005 **FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/SG2005/000067	3 March 2005	3 March 2004

International Patent Classification (IPC) or both national classification and IPC
Int. Cl. [7] H01L 25/065, 23/48

Applicant
UNITED TEST AND ASSEMBLY CENTER LIMITED et al

1. This opinion contains indications relating to the following items:

- [X] Box No. I — Basis of the opinion
- [ ] Box No. II — Priority
- [ ] Box No. III — Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV — Lack of unity of invention
- [X] Box No. V — Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [X] Box No. VI — Certain documents cited
- [ ] Box No. VII — Certain defects in the international application
- [X] Box No. VIII — Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the IPEA/AU	Authorized Officer
AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	**GREG POWELL** Telephone No. (02) 6283 2308

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Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material

      ☐ in written format

      ☐ in computer readable form

   c. time of filing/furnishing

      ☐ contained in the international application as filed.

      ☐ filed together with the international application in computer readable form.

      ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

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Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-31	YES
	Claims		NO
Inventive step (IS)	Claims		YES
	Claims	1-31	NO
Industrial applicability (IA)	Claims	1-31	YES
	Claims		NO

2. Citations and explanations:
The following documents identified in the International Search Report have been considered for the purposes of this report:

D1 US 6107109
D2 US 5222014
D3 US 2002/0027295
D4 EP 1355352
D5 US 2002/0149097

NOVELTY (N)

No individual document discloses all the features of claim 1. It is novel. As claims 2-31 are ultimately dependent on claim 1, they are also novel.

INVENTIVE STEP (IS)

Claim 1

D1 discloses (see figure 9A) a semiconductor device having a two chips (20E) mounted upon two different substrates (130A) having areas where the chips can be mounted. Each substrate carries terminals (36D) and conductive traces (138) and has an opening (136). Claim 1 differs from D1 in that there is no explicit disclosure in D1 of the use of adhesives and encapsulating. However, it is common general knowledge in the art to encapsulate devices and to use adhesives to mount chips to substrates. These differences add no inventive step. There is a further difference between claims 1 and what is shown in figure 9A of D1 in that the last semiconductor chip does not have its electrically inactive side mounted to the intermediate substrate. Rather the presence of the window in this substrate allows the chip's electrically active side to be mounted to the substrate. However, as is shown in figure 9B of D1, there is clear suggestion that the chip can be mounted with its electrically active side uppermost. This difference is a mere workshop variation adding no inventive step.

Claims 2-31

The features of these claims are either disclosed in D1 (e.g. claims 2, 15, 16, etc), are common general knowledge in the art (e.g. claims 6-10, 12-14, etc), are mere workshop variations (e.g. claims 3, 4, etc) or represent mere choices to be made by the person skilled in the art (e.g. claims 11, 17, etc). As such, they add no inventive step, and are anticipated by D1.

(continued)

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Box No. VI Certain documents cited

1. Certain published documents (Rules 43*bis*.1 and 70.10)

Application No. Patent No.	Publication date *(day/month/year)*	Filing date *(day/month/year)*	Priority date (valid claim) *(day/month/year)*
P, X US 2004/0159954	19 August 2004	17 December 2003	17 December 2002
P, X WO 2004/088727	14 October 2004	2 April 2004	2 April 2003

Each of these documents clearly discloses (see their figures) mounting chips on substrates with openings. Any features not disclosed are either common general knowledge, mere workshop variations or mere choices adding no inventive step.

2. Non-written disclosures (Rules 43*bis*.1 and 70.9)

Kind of non-written disclosure	Date of non-written disclosure *(day/month/year)*	Date of written disclosure referring to non-written disclosure *(day/month/year)*

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Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

1. Claim 1 is not fully supported by the description. It is clear from the description that the last semiconductor die is only ever directly electrically connected to the second substrate. However, the claim defines electrically connecting the last semiconductor die to "said conductive traces of said first or second substrate directly". Connecting the last die to the first substrate is not disclosed.

   Furthermore, claim 1 defines transferring electrical signals to the exterior of the package via the conductive traces, but does not limit those traces to the ones which are formed on the first substrate. There is no other arrangement disclosed.

   In addition, in the invention defined in claim 1, there seems to be no reason for the provision of the window. As such it appears to make no technical contribution to the invention and should be deleted.

2. Claim 7 makes claim 8 redundant.

3. Claim 15 appears to be a claim that was meant to be appended to an earlier claim, however, no claim appendency is given. For the purposes of this opinion I have assumed that claim 15 was appended to claim 1. However, if claim 15 was meant to be an independent claim, it is not supported by the description because it is missing many features which are clearly set out as being part of the invention.

4. Claim 22 is not clear because I cannot find an antecedent to "the interconnection" when the claim is appended to Claim 1.

5. Claim 23 is not fully supported by the description because there is no disclosure that a semiconductor die located between the first and last dies is electrically coupled to the first substrate. The only disclosure is of electrically coupling these dies to the second substrate.

6. Claim 25 is not clear because it is not clear where in the stack the spacer is positioned. This is particularly so when there are more than two semiconductor dies.

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Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of **Box V**:

Claims 1-31

Notwithstanding the above, these claims lack an inventive step. D2-D4 each disclose (see their figures) mounting one chip on a first substrate, placing an intermediate substrate above the first chip, mounting a second chip on the intermediate substrate and electrically coupling the chips and the substrates. D2-D4 do not disclose the substrates as having openings in them. However, it is clear from D5 that it is known in multichip modules to mount chips on substrates with holes in them. The combination of D5 with any one of D2-D4, as would be obvious to a person skilled in the art since they are all located in the same art, anticipates claims 1-31. Any features not disclosed by this combination are either common general knowledge, mere workshop variations or mere choices adding no inventive step.